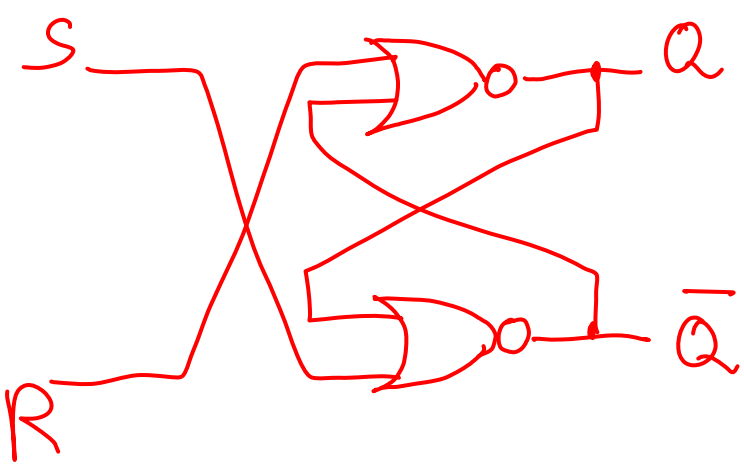
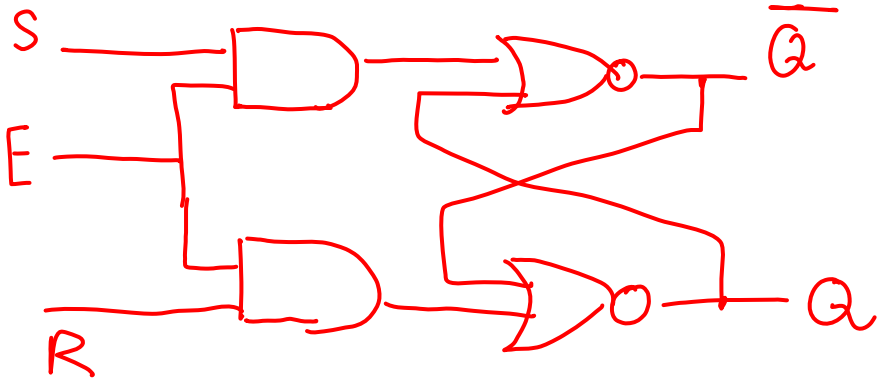
Inside of RS FF's

NOR gate RS latch



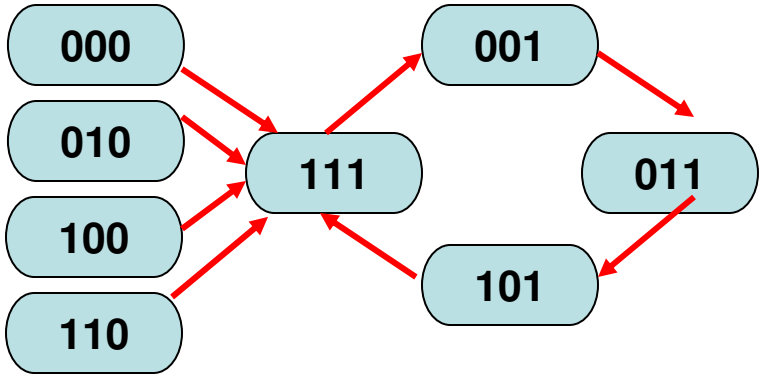
S	R	Q	$\bar{Q}$	
1	0	1	0	
0	1	1	0	→ unstable
0	0	1	0	} two possibilities
		0	1	
1	1	undetermined		

With Enable



Sequential Logic Design

- **State Diagram (State transition table):** A Case Study: design an 3-bit counter that only counts 1,3,5,7 using D FF
- How many outputs do we need? 3 (encode the states)

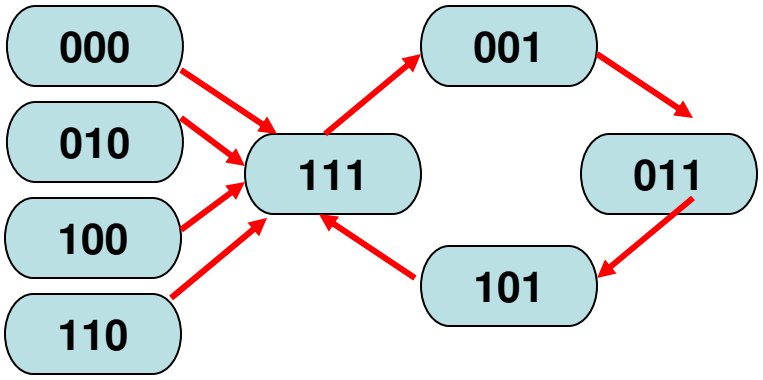


Truth Table

Q_3	Q_2	Q_1	D_3	D_2	D_1
0	0	1	0	1	1
0	1	1	1	0	1
1	0	1	1	1	1
1	1	1	0	0	1
0	0	0	1	1	1
0	1	0	1	1	1
1	0	0	1	1	1
1	1	0	1	1	1

- For unused states, usually reset to 000, or 111, or if not particularly required, can be labeled as d (don't care) (or x)
- Construct the truth table: write down current state ($Q_1Q_2Q_3$•••) and use current state to prepare the inputs of FF's to go into the next state specified in the state diagram.
  - Outputs of FF's (Q1Q2Q3•••) are inputs in the truth table, inputs of FF's ($D_1D_2D_3$•••) are outputs in the truth table.
- Use Karnaugh map to design the circuit

Sequential Logic Design



Red supercell: Q_1'
Green supercell: Q_2'

Draw circuit

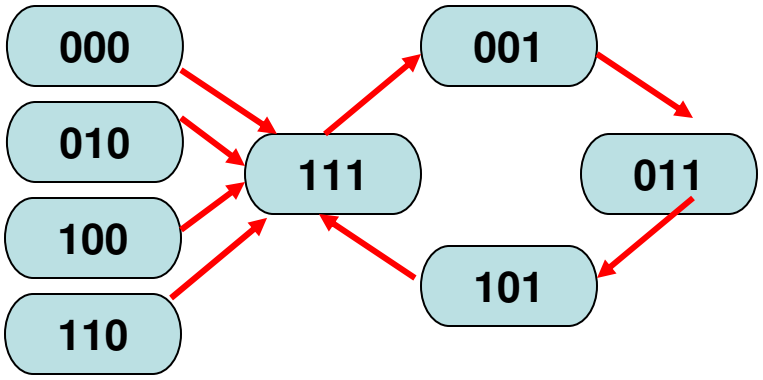
Truth Table

Q_3	Q_2	Q_1	D_3	D_2	D_1
0	0	1	0	1	1
0	1	1	1	0	1
1	0	1	1	1	1
1	1	1	0	0	1
0	0	0	1	1	1
0	1	0	1	1	1
1	0	0	1	1	1
1	1	0	1	1	1

The Karnaugh map for D_2 is:

	Q_1	0	1
Q_3Q_2			
00		1	1
01		1	0
11		1	0
10		1	1

Sequential Logic Design



Red supercell: Q_1'
Green supercell: Q_2Q_3'
Gray supercell: $Q_2'Q_3$
D_1: $Q_1'+Q_2Q_3'+Q_2'Q_3$
D_2: $Q_1'+Q_2'$
D_3: 1

Draw circuit with CLK.
Real Applications:
- **odd number generator**
- **B-game score counter: CLK is input**

Truth Table

Q_3	Q_2	Q_1	D_3	D_2	D_1
0	0	1	0	1	1
0	1	1	1	0	1
1	0	1	1	1	1
1	1	1	0	0	1
0	0	0	1	1	1
0	1	0	1	1	1
1	0	0	1	1	1
1	1	0	1	1	1

The Karnaugh map for D_3 is:

	Q_1	0	1
Q_3Q_2			
00		1	0
01		1	1
11		1	0
10		1	1

D_1 : $\overline{Q_1} + Q_2 \cdot \overline{Q_3} + \overline{Q_2} \cdot Q_3$

D_2 : $\overline{Q_1} + \overline{Q_2}$

D_3 : 1